control – motion – interface

IT 251

Level Converter and Programmable Impulse Divider

- Level conversion from TTL / RS 422 to HTL 10 … 30 V and vice versa
- Programmable divider for error- free and position-true division of quadrature encoder Signals (A / B / 90°)
- Separate marker pulse divider with individual settings
- 300 kHz of maximum frequency
- Push-pull outputs for direct PLC interfacing
- Single 18 … 30Vdc supply

Operating Instructions

Safety Instructions

- This manual is an essential part of the unit and contains important hints about function, correct handling and commissioning. Non-observance can result in damage to the unit or the machine or even in injury to persons using the equipment!

- The unit must only be installed, connected and activated by a qualified electrician

- It is a must to observe all general and also all country-specific and application-specific safety standards

- When this unit is used with applications where failure or maloperation could cause damage to a machine or hazard to the operating staff, it is indispensable to meet effective precautions in order to avoid such consequences

- Regarding installation, wiring, environmental conditions, screening of cables and earthing, you must follow the general standards of industrial automation industry

- - Errors and omissions excepted –

| Version:	Description:
It25101e/ TJ/ Sep 03/5	HTL input circuit resistors
It25102a/ hk/ Jan07	Brochure format, improved clarification of functions

Table of Contents

1. Introduction

IT 251 has been designed as a universal encoder interface for use with incremental encoder signals. The unit is suitable to solve the following applications:

- Level conversion from TTL / RS422 to HTL and vice-versa
- Division of quadrature encoder pulses, with adjustable division rate from 1:1 to 1:4096
- Separately programmable division of the marker pulses
- Translation from any of the three common standards of indication of the direction to any other standard (quadrature A/B 90° or A = pulse and B = direction or A = forward impulse and B = reverse impulse)

All settings occur from the top or bottom side of the unit, by means of four 8-position DIL switches.

The unit is built into a compact housing with 12 screw terminals and two Sub-D-connectors and can be mounted to DIN rails

2. Block Diagram
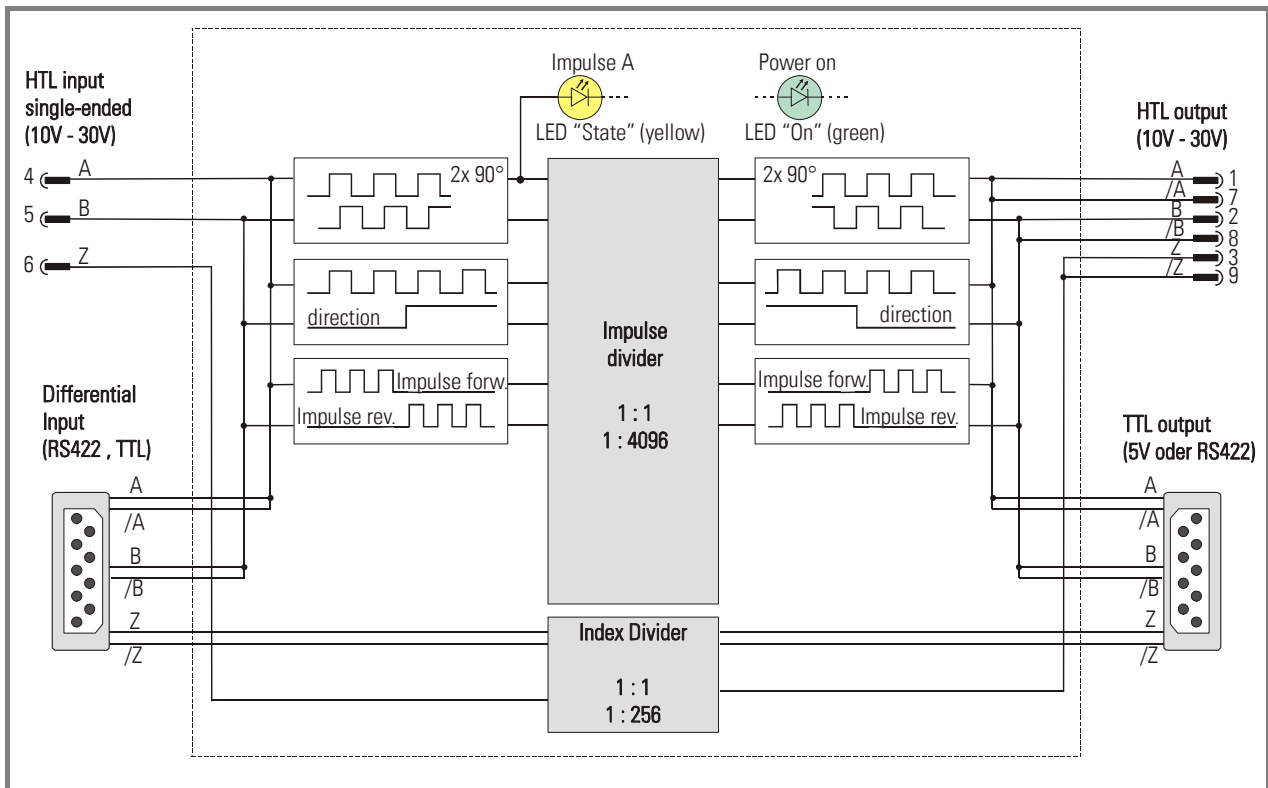
3. Connections and Terminal Assignments

For frequency input, either the RS 422 inputs (D-SUB) or the 10 – 30 V HTL inputs can be used. The other inputs, which are not in use, must remain unconnected or must be disabled by corresponding DIL switch setting.

The outputs provide impulse signals at TTL / RS422 level as well as at a 10 – 30 V HTL level, and either one or the other or both at a time can be used, whichever is applicable.

Please note that all input and output signals refer to the same common potential (GND) which at the same time is also the minus potential of the power supply.
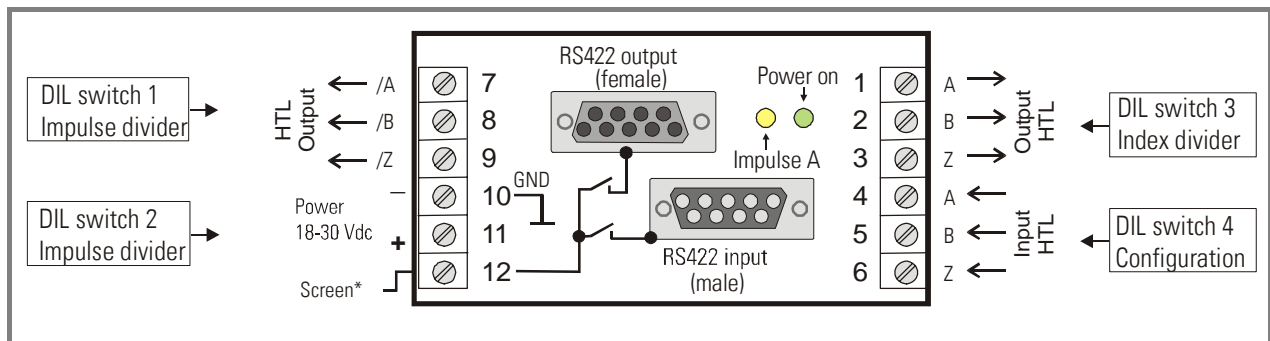
*) This screen terminal allows to connect the metallic housings of the SUB-D-connectors to the potential applied to terminal 12 (e.g. PE or external GND or else), when the corresponding DIL switch is on (see settings of DIL 4 switch)

The D-SUB input connector provides an auxiliary output of +5 V / 130 mA for encoder supply.

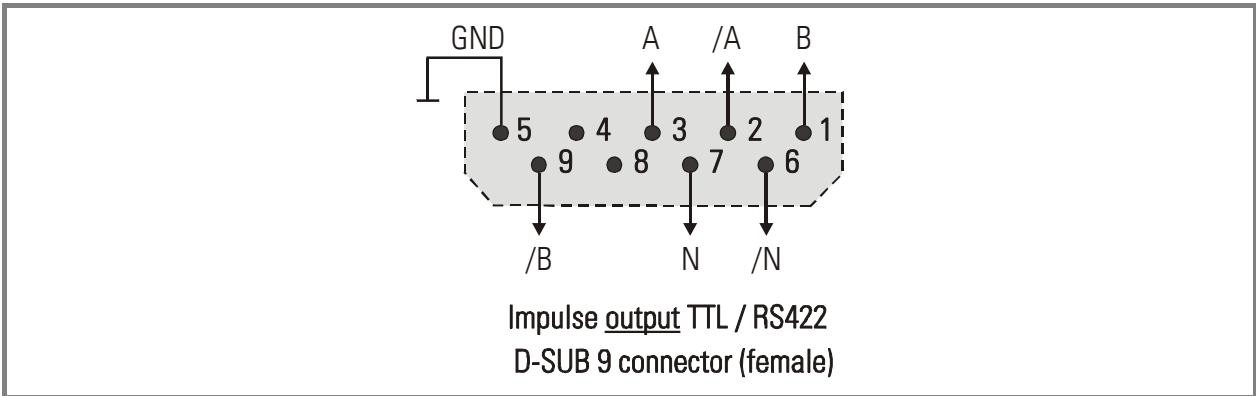The **HTL inputs** provide PNP characteristics and must be switched to +.
Where you use encoders with PNP or push-pull outputs, there will be no problem.

Encoders with NPN outputs (open collector type) will however need an external pull-up resistor (e.g. 2.7 kOhms). See the schematics of the input circuit for calculation of the resistance.

At any time, the total transmission characteristics of encoder, external components and capacity of the cable must ensure proper signals at the input terminals of the unit, with respect to the levels, the shape and the phase displacement A/B.

The output swing on the HTL push- pull outputs corresponds to the input supply voltage applied to terminals 10 and 11.

The green front LED signals that power is on, and the yellow LED signals the input impulses from input channel A respectively A, /A.

HTL input
Low < 4.0 V
High > 9.0 V

2.7 k

6 k

Vref = 5.5 V

-

+

Typical input circuit of HTL inputs

B   /A   A   +5.5V   GND

1   2   3   4   5
6   7   8   9

/N   N   /B

Impulse input TTL / RS422
D-SUB 9 connector (male)

GND   A   /A   B

5   4   3   2   1
9   8   7   6

/B   N   /N

Impulse output TTL / RS422
D-SUB 9 connector (female)
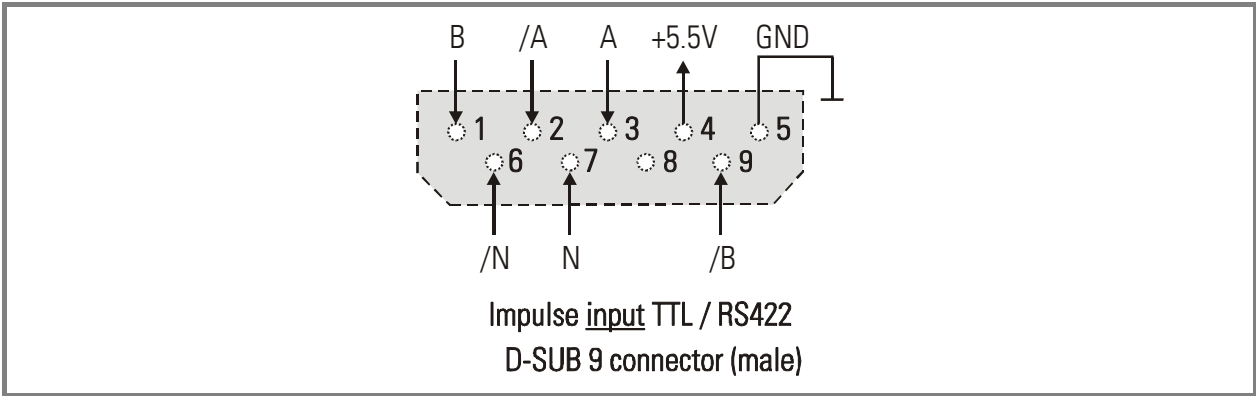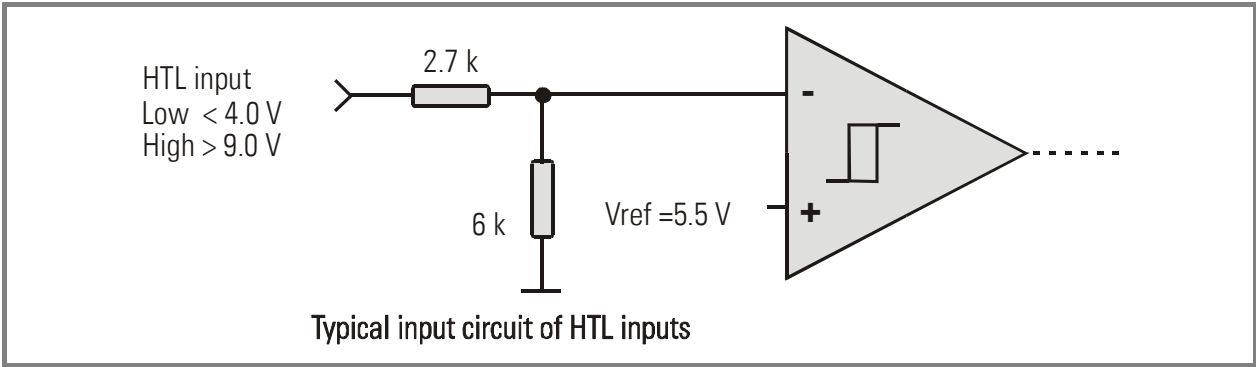
4. Basic Switch Settings

Upon commissioning, some basic settings must be done by switch **DIL4.**
These settings select one of the possible standards for expressing the direction of rotation on inputs and outputs. Also the potential of the metallic housings of the SUB-D-connectors can be set, and the inputs can be enabled or disabled (RS422 signals or HTL signals)

Changes of the DIL switch positions will become active
only after the next power-up of the unit!
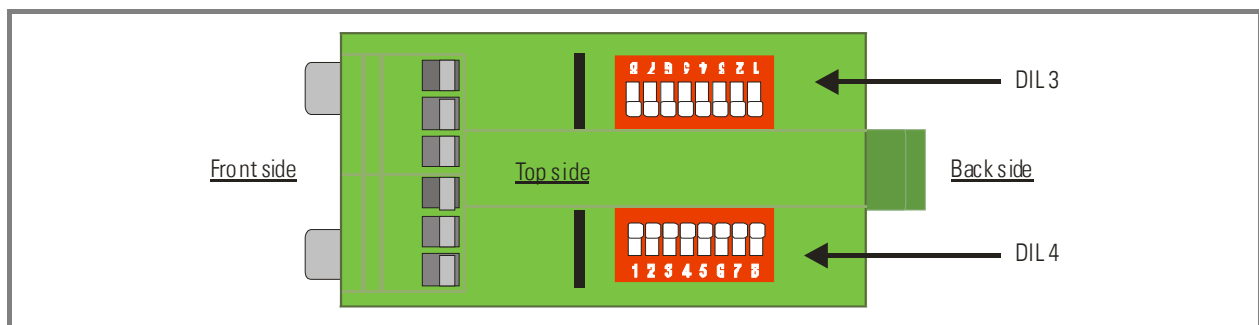
DIL switches **DIL3** and **DIL4** are located on the top side and switches **DIL1** and **DIL2** are located on the bottom side of the unit.

Configuration										
DIL4										
8	7	6	5	4	3	2	1			
						on	on	2x 90° A B	1**	Output direction standard
						on	off	A Impulse forw. Impulse rev. B	2	
						off	on	A Direction B	3	
					on	on		2x 90°	1	Input direction standard
					on	off		A Impulse forw. Impulse rev. B	2*	
					off	on		A Direction B	3*	
			on					Connects the metallic housing of SUB-D-connector "RS422 Input" to terminal 12		
			off					Metallic housing of the SUB-D-connector "RS422 Input" is potential-free		
		on						Connects the metallic housing of SUB-D-connector "RS422 Output" to terminal 12		
		off						Metallic housing of the SUB-D-connector "RS422 Output" is potential-free		
	on							HTL Inputs disabled		
	off							HTL Inputs enabled		
on								TTL / RS422 Inputs disabled		
off								TTL / RS422 Inputs enabled		

*) Where your application uses input format 2 or 3 to indicate the direction, you should ensure that changes of direction occur always while the pulse lines are low. Otherwise there is a risk of cumulating error pulses at the output with frequent changes of direction.

) Also from input signals according to direction standards 2 or 3, the unit can generate a quadrature output with A/B phase displacement, according to direction standard 1. However, with the divider set to **1:1, the phase displacement then is <u>constant in time</u>, i.e. the phase between A and B

corresponds to 90° only at a certain input frequency, and becomes smaller with lower input frequencies. This, in general, is not a restriction for proper detection of the direction, because practically every counter or position controller can clearly interpret this information, even when the phase is barely visible on an oscilloscope.

For this kind of application, please set the A/B delay time by DIL switch 2, with consideration of your maximum output frequency.

For division rates higher than 1:1, the phase displacement gets more and more close to a real 90° quadrature signal, independent of the input frequency.

A/B time displacement when converting
direction standard 2 or 3 to quadrature standard
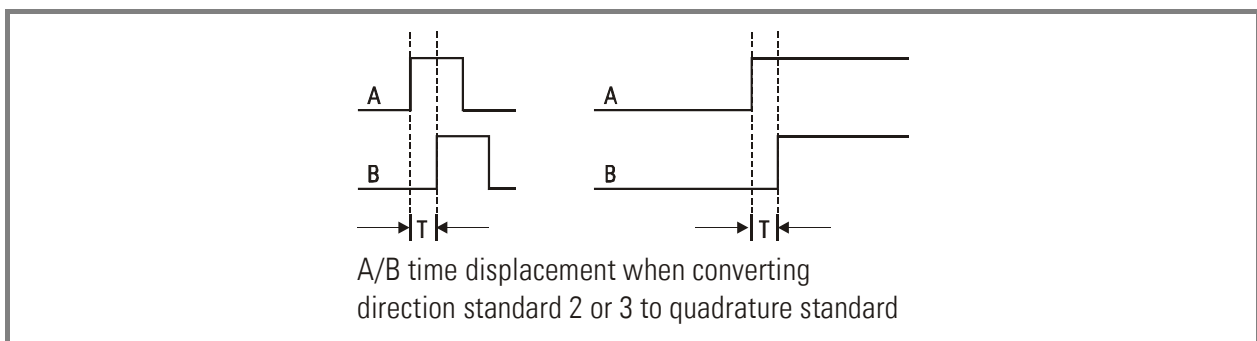
A/B Time Displacement		
DIL2		
8	7	
on	on	T = 0,4 µs
on	off	T = 1,2 µs
off	on	T = 4,4 µs
off	off	T = 10,0 µs

5. Setting of the Impulse Division Rate

The incremental division rate for the A/B input pulses can be set by means of switch **DIL1** and by positions 1 – 4 of switch **DIL2**.
The marker pulse Z uses a separate divider and marker division is described later.

The switch positions use a binary code like shown in the subsequent list. For technical reasons, a switch in <u>ON position means logical "0"</u> and a switch <u>in OFF position means logical "1"</u>.
Set all switch positions to a binary code that corresponds to the <u>desired division rate – 1</u>

Impulse Divider [A / B]												
DIL2				DIL1								on = log.0, off = log.1
4	3	2	1	8	7	6	5	4	3	2	1	← —— Binary value
2048	1024	512	256	128	64	32	16	8	4	2	1	
on	on	on	on	on	on	on	on	on	on	on	on	(0) = Division 1 : 1
on	on	on	on	on	on	on	on	on	on	on	off	(1) = Division 1 : 2
on	on	on	on	on	on	on	on	on	on	off	on	(2) = Division 1 : 3
on	on	on	on	on	on	on	on	on	on	off	off	(3) = Division1 : 4
on	on	on	on	on	on	on	on	on	off	on	on	(4) = Division 1 : 5
on	on	on	on	on	on	on	on	on	off	on	off	(5) = Division 1 : 6
on	on	on	on	on	on	on	on	on	off	off	on	(6) = Division 1 : 7
on	on	on	on	on	on	on	on	on	off	off	off	(7) = Division 1 : 8
												...etc.
on	on	on	on	on	on	on	off	on	on	on	on	1 : 17
on	on	on	on	on	on	off	on	on	on	on	on	1 : 33
on	on	on	on	on	off	on	on	on	on	on	on	1 : 65
on	on	on	on	off	on	on	on	on	on	on	on	1 : 129
on	on	on	off	on	on	on	on	on	on	on	on	1 : 257
on	on	off	on	on	on	on	on	on	on	on	on	1 : 513
on	off	on	on	on	on	on	on	on	on	on	on	1 : 1025
off	on	on	on	on	on	on	on	on	on	on	on	1 : 2049
												...etc.
off	off	off	off	off	off	off	off	off	on	off	off	1 : 4092
off	off	off	off	off	off	off	off	off	off	on	on	1 : 4093
off	off	off	off	off	off	off	off	off	off	on	off	1 : 4094
off	off	off	off	off	off	off	off	off	off	off	on	1 : 4095
off	off	off	off	off	off	off	off	off	off	off	off	1 : 4096

6. Index Pulse Divider (Marker Pulse Z)

6.1. Unchanged index pulse (bypass)

When you like to just bypass the index pulse from the input to the output (without any changes of frequency, position and pulse width), please use the following DIL switch settings:

DIL3									DIL2	
8	7	6	5	4	3	2	1		6	5
on	on	on	on	on	on	on	on		off	off

In this case you can ignore all further information given in this chapter.

6.2. Modifications of the index pulse

The programmable index divider allows modifications of the pulse distance, the pulse width and the pulse position.

As a precondition for use of the subsequent functions, the input index pulse needs to have a

minimum width of one fourth of the period and a maximum width of one half of the period of the input frequency
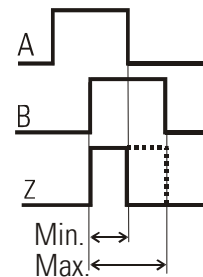
Switch DIL3 allows setting of the division rate between input and output.

Positions 5 and 6 of switch DIL2 allow modification of width and position of the output pulse.
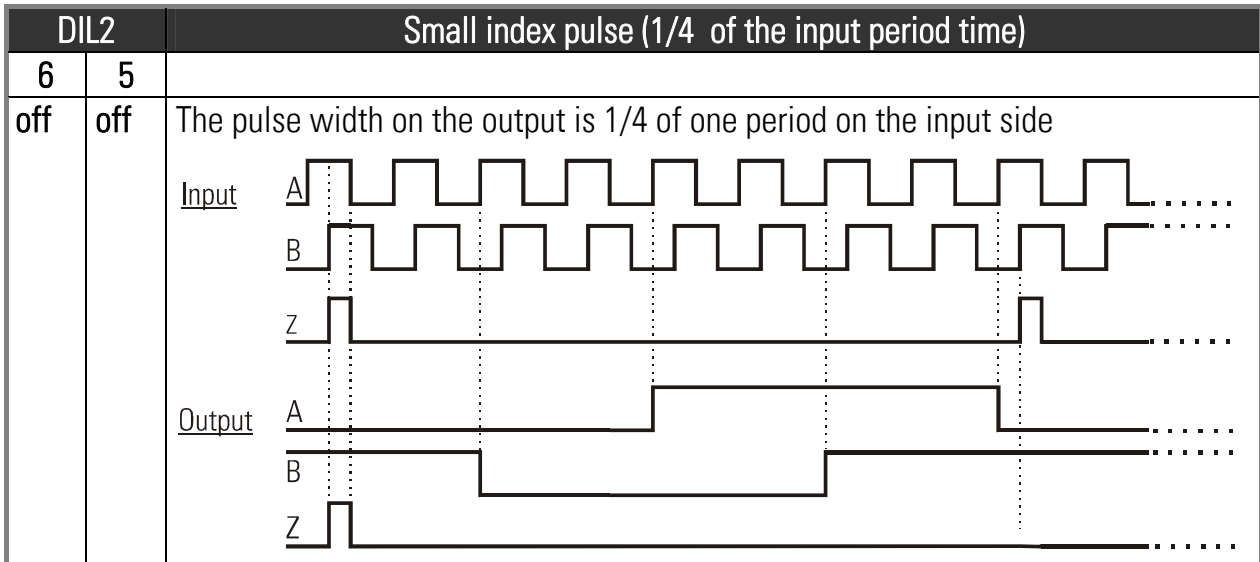
6.3. Setting of the division rate of the index divider

These settings use the same rules and codes as shown with the main divider (see section 5)

Index Divider [Z]								
DIL3								on = log.0, off = log.1
8	7	6	5	4	3	2	1	
128	64	32	16	8	4	2	1	← Binary value
on	on	on	on	on	on	on	on	1 : 1
on	on	on	on	on	on	on	off	1 : 2
on	on	on	on	on	on	off	on	1 : 3
on	on	on	on	on	on	off	off	1 : 4
off	off	off	off	off	off	on	on	1 : 253
off	off	off	off	off	off	on	off	1 : 254
off	off	off	off	off	off	off	on	1 : 255
off	off	off	off	off	off	off	off	1 : 256

6.4. Position and width of the index pulse

For illustration of the functions, the drawings of this chapter assume that the main impulse divider of the A/B input pulses would be set to 8. The index pulse will appear at the output according to the division rate set under 6.3

DIL2		Small index pulse (1/4 of the input period time)
6	5	
off	off	The pulse width on the output is 1/4 of one period on the input side

DIL2		Enlarged index pulse (one full encoder revolution)
6	**5**	
off	on	The pulse width of the enlarged output index pulse corresponds to the distance between two input index pulses (with index divider > 1 only).

DIL2		Index pulse width adapted to output frequency (1/4 output period) (only applicable with quadrature input A/B, 90°)
6	**5**	
on	off*)	The pulse width corresponds to 1/4 of one period of the output frequency
on	on**)	
	☞	This mode of index treatment requires divider settings of the A/B impulse divider and the index divider that ensure a clear assignment of the output index pulse to the A/B output frequency, with no cumulating remainders. Where the signal division does not come out even, jumps of the output index pulse position will occur. Example: With use of a 1000 ppr encoder we would set the A/B impulse divider to 3 and the index divider to 2. As a result the index output pulse should appear after every 666.6….. input pulses, what physically is impossible without jumps. *) Pulse width = 1/4 output period, even with index divider set to 1:1 **) Divider setting 1:1 will bypass the input index pulse to the output

7.   Technical Data and Dimensions

Power supply (without load)	:	18 Vdc (0.25 A) – 30 Vdc (0.15 A)
Aux. output for encoder supply	:	5.5 V / max. 130 mA
Max. input frequency	:	300 kHz
Output swing on HTL outputs	:	17...29 V (depending on power supply)
Max. current HTL outputs	:	20 mA (push-pull)
HTL input levels	:	$V_{LOW} < 5$ V, $V_{HIGH} > 10$ V
HTL input resistance	:	approx. 5 kΩ
Operating temperature	:	0...+45 °C / 32...110 °F
Weight	:	approx. 200 g

Conformity and Standards	:	EMC 89/336/EEC :	EN 61000-6-2
			EN 61000-6-3
		LV73/23/EEC :	EN 61010-1

Front view   40 mm (1.575'')   79 mm (3.110'')

Side view   91mm (3.583'')   74 mm (2.193'')